## REMARKS

Applicants respectfully request reconsideration of the present application in view of the foregoing amendments and the following remarks. Claims 11 and 12 have been amended to clarify the invention. Claims 1-17 remain pending in the application.

In the Office Action dated May 20, 2004, the Examiner rejected claims 11 and 12 under 35 U.S.C. 112 as failing to particularly point out and distinctly claim the invention Applicants respectfully submit that the rejection of claims 11 and 12 should be withdrawn in light of the amendments submitted herein.

The Examiner also rejected claims 1-10 and 12-17 under 35 U.S.C. 102(b) as being anticipated by Chang et al. ("Chang"). Anticipation of a claim requires that each and every element of that claim be disclosed by a single reference. Applicants respectfully traverse the anticipation rejection of claims 1 and 16 because Chang does not disclose the step of "testing microcode by using a hardware emulator behaving in the same way as the hardware of said processor according to the design of the processor's logic gates."

Fig. 6 in Chang illustrates the entire system for verifying a processor design. The verification process is clearly split into two main processes: microcode verification and RTL verification. Applicants understand the term "RTL" to mean Register Transfer Level. See http://www.vlsi.wpi.edu/FPGA_Manual/node11.html. While the term was not defined in Chang, the aforementioned web reference provides that RTL verification refers to a testing of the processor logic without delays. RTL verification is clearly different from microcode verification based on the definition of RTL verification and also because, as clearly shown in Figure 6, the two verification processes are split, meaning that they are not one and the same process.

Chang does not elaborate on the specific means to verify the microcode. Instead, Chang focuses and describes the RTL verification process by use of (1) HDL in the RTL simulation and (2) an emulator. See section 4 in Chang. Because the emulation function in Chang is only applied as part of the RTL verification process and not to microcode verification, Chang does not disclose "testing the microcode by using a hardware emulator" as required by claims 1 and 16. Consequently, Chang does not disclose each and every element of those claims. For the foregoing reasons,

Applicants respectfully request that the rejection of those claims be withdrawn. Further, the rejection of claims 2-10 and 12-15 should also be withdrawn at least by virtue of their dependency from claim 1.

Claim 17 recites a system that includes an emulator for performing the step discussed above in connection with the patentability of claims 1 and 16. Therefore, Applicants respectfully submit that the rejection of claim 17 should be withdrawn at least for the reasons set forth above in connection to the patentability of claims 1 and 16.

Claim 11 was rejected by the Examiner under 35 U.S.C. 103 as being rendered obvious by Chang. Obviousness requires that the combination of references teach or suggest all of the elements in the claim being examined. Applicants respectfully traverse the rejection of claim 11 because that claim incorporates by reference the elements of claim 1 that Chang fails to disclose, as pointed out in the discussion above. Therefore, Applicants respectfully request that the rejection of claim 11 be withdrawn.

In view of the foregoing, Applicants earnestly solicit the expedited allowance of the pending claims. The Commissioner is hereby authorized to charge any fee(s) necessary to enter this paper and any previous paper, or credit any overpayment of fees to deposit account 09-0468.

Respectfully submitted,

By: _____

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